Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	4	fpga same prototyp$3 same pin same count$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 16:25
S2	120	(fpga or pld) same prototyp$3 and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 16:26
S3	0	(fpga or pld) same prototyp$3 same ((COM adj wrapper) or (convert$3 near3 data near3 signal)) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 16:28
S4	2	(fpga or pld) same prototyp$3 and ((COM adj wrapper) or (convert$3 near3 data near3 signal)) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/30 16:30
S5	17	(fpga or pld) same prototyp$3 and ((COM adj wrapper) or (convert$3 near3 data near3 signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:10
S6	13	(fpga or pld) and ((COM adj wrapper) or (convert$3 near3 data near3 signal)) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:16
S7	4	(fpga or pld) same ((COM adj wrapper) or (convert$3 near3 data near3 signal)) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:20
S8	71	(fpga or pld) same ((COM adj wrapper) or (convert$3 near3 data near3 signal))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:41
S9	14	(fpga or pld) same ((COM adj wrapper) or (convert$3 near3 data near3 signal)) same asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:38
S10	14	(fpga or pld) same (((COM or interconnect) adj wrapper) or (convert$3 near3 data near3 signal)) same asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:40

S11	14	(fpga or pld) same (((COM or interconnect) adj wrapper) or (convert$3 near3 data near3 signal) or serialz$3) same asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 08:41
S12	354211	asic fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic) same pin same (($3mux $3multiplexor) serial$5 swithc$3 ceossbar) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 09:42
S13	354212	asic fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic) same pin same (($3mux $3multiplexor) serial$5 switch$3 ceossbar) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 09:42
S14	354212	asic fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic) same pin same (($3mux $3multiplexor) serial$5 switch$3 crossbar) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 09:57
S15	147	(asic fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic)) same pin same (($3mux $3multiplexor) serial$5 switch$3 crossbar) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 09:57
S16	9	(asic same (fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic))) same pin same (($3mux $3multiplexor) serial$5 switch$3 crossbar) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 10:07
S17	19	(asic fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic)) SAME (PIN SAME ($3MUX $3MULTIPLEXOR)) AND "716"/$.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 10:11
S18	47	(asic fpga (application near3 specific) (filed near3 programmable) pld plc pla (programmable near3 logic)) SAME (PIN SAME ($3MUX $3MULTIPLEXeR)) AND "716"/$.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 10:53
S19	49	com adj wrapper	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 10:57
S20	17431	((com near3 (wrapper or interface)) or (convert$3 same parallel same singal same serial same data) or serial$5 or switch$3 or crossbar) same (fpga asic pld pla plc)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:06

S21	521	((com near3 (wrapper or interface)) or (convert$3 same parallel same singal same serial same data) or serial$5 or switch$3 or crossbar) same (fpga asic pld pla plc) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:06
S22	61	((com near3 (wrapper or interface)) or (convert$3 same parallel same singal same serial same data) or serial$5 or switch$3 or crossbar) same (fpga asic pld pla plc) same (block or part or partition$3) same pin and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:14
S23	7	((com near3 (wrapper or interface)) or (convert$3 same parallel same singal same serial same data) or serial$5 or switch$3 or crossbar) same (fpga asic pld pla plc) same (block or part or partition$3) same pin same count$3 and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:19
S24	7	((com near3 (wrapper or interface)) or (convert$3 near3 parallel near3 singal near3 serial near3 data) or serial$5 or switch$3 or crossbar) same (fpga asic pld pla plc) same (block or part or partition$3) same pin same count$3 and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:21
S25	7	((com near3 (wrapper or interface)) or (convert$3 near3 parallel near3 signal near3 serial near3 data) or serial$5 or switch$3 or crossbar) same (fpga asic pld pla plc) same (block or part or partition$3) same pin same count$3 and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:36
S26	4	(convert$3 near3 parallel near3 signal near3 serial near3 data) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:52
S27	0	(convert$3 near3 parallel near3 signal near3 serial near3 data) and serializer and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:49
S28	34	(convert$3 same parallel same signal same serial same data) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:55
S29	0	convert$3 same parallel same signal same serial same data same (asic or fpga or pld or plc or pla) same pin and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 11:56

S30	2	convert$3 same parallel same signal same serial same data same (asic or fpga or pld or plc or pla) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:12
S31	2	convert$3 same (parallel near3 signal) same (serial near3 data) same (asic or fpga or pld or plc or pla) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 12:47
S32	3	(parallel near3 signal) same (serial near3 data) same (asic or fpga or pld or plc or pla) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:18
S33	3	convert$3 same parallel same signal same serial same data same (asic or fpga or pld or plc or pla or pll) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:13
S34	5	(parallel near3 signal) same (serial near3 data) same (asic or fpga or pld or plc or pla or pll or (programmable adj logic)) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:47
S35	0	(parallel adj output adj signal) same (serial adj data adj stream) same (fpga or pld or plc or pla or pll) same pin same count and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:50
S36	0	(parallel adj output adj signal) same (serial adj data adj stream) same (fpga or pld or plc or pla or pll) same pin same count	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:50
S37	0	(parallel adj output adj signal) same (serial adj data adj stream) same (fpga or pld or plc or pla or pll) same pin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:51
S38	0	(parallel adj output adj signal) same (serial adj data adj stream) same (fpga or pld or plc or pla or pll or asic) same pin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:51
S39	0	(parallel adj output adj signal) same (serial adj data adj stream) same (fpga or pld or plc or pla or pll or asic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:52

S40	0	(parallel near3 output near3 signal) same (serial near3 data near3 stream) same (fpga or pld or plc or pla or pll or asic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 14:52
S41	25	(parallel near3 output near3 signal) same (serial near3 data) same (fpga or pld or plc or pla or pll or asic)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:32
S42	2	asic same partition$3 same serializer same deserializer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:37
S43	1407	asic same (partition$3 or block or part or subcircuit or (sub adj circuit)) same (serializer or deserializer or parallel or serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:37
S44	45	asic same (partition$3 or block or part or subcircuit or (sub adj circuit)) same (serializer or deserializer or parallel or serial) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 16:44
S45	111	asic same partition$3 and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:37
S46	1848	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) and (serializer or deserializer or parallel or serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:38
S47	1851	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) and (serializ$3 or deserializ$3 or parallel or serial)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:38
S48	225	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) and (serializ$3 or deserializ$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:44
S49	3	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) and (serializ$3 or deserializ$3) and "716"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:39

S50	1	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) same (fpga or pld or pll or pls or pla) and (serializ$3 or deserializ$3) and (convert$3 same parallel same serial same signal same data)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:49
S51	8	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) same (fpga or pld or pll or pls or pla) and (serializ$3 or deserializ$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:53
S52	219	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) same (fpga or pld or pll or pls or pla)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/01 17:53
S53	5	(asic near3 (partition$3 or block or part or subcircuit or (sub adj circuit))) same (fpga or pld or pll or pls or pla) same pin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 07:44
S54	2	"20020095649"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 07:15
S55	13339	(pld fpga) same asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 07:45
S56	0	(pld fpga) same asic same pin same (serializer or desirializer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 07:46
S57	29	(pld fpga) same asic same pin and (serializer or desirializer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 08:20
S58	151	(pld fpga) same asic and (serializer or desirializer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 08:20
S59	17	(pld fpga) same asic same (serializer or desirializer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 08:21

S60	2	"20040060032"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/08 18:41

Results for **"((asic and (fpga or pld or pla programmable) and (convert or serial*)) <in>metadata)"**
Your search matched **24** of **1278046** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

☐ **1. FPGA-based FIR filters using digit-serial arithmetic**
Hanho Lee; Sobelman, G.E.;
ASIC Conference and Exhibit, 1997. Proceedings., Tenth Annual International
7-10 Sept. 1997 Page(s):225 - 228
Digital Object Identifier 10.1109/ASIC.1997.617010
AbstractPlus | Full Text: PDF(372 KB) **IEEE CNF**

☐ **2. Development of reusable serial FIR filters with reprogrammal coefficients designed for serial dataflow architectures**
Adaos, K.; Alexiou, G.; Kanopoulos, N.;
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IE International Conference on
Volume 1, 17-20 Dec. 2000 Page(s):567 - 570 vol.1
Digital Object Identifier 10.1109/ICECS.2000.911603
AbstractPlus | Full Text: PDF(312 KB) **IEEE CNF**

☐ **3. ASIC vs. programmable logic devices (PLDs) for low comple**
Young, M.S.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annua International
23-27 Sept. 1991 Page(s):P16 - 1/1-4
Digital Object Identifier 10.1109/ASIC.1991.242884
AbstractPlus | Full Text: PDF(244 KB) **IEEE CNF**

☐ **4. Bit-serial digital filter architecture using RAM-based delay o**
Bull, D.R.; Wacey, G.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE P Circuits, Devices and Systems]
Volume 141, Issue 5, Oct. 1994 Page(s):371 - 376
AbstractPlus | Full Text: PDF(396 KB) **IEE JNL**

☐ **5. FPGA to ASIC conversion design methodology with the supp retargetting to different CMOS implementation technologies**
Markovic, P.; Mujkovic, V.;

Microelectronics, 2000. Proceedings. 2000 22nd International Co
Volume 2, 14-17 May 2000 Page(s):703 - 706 vol.2
Digital Object Identifier 10.1109/ICMEL.2000.838787
AbstractPlus | Full Text: PDF(144 KB) **IEEE CNF**

☐ **6. Migration from FPGA to gate array**
Zhao Li;
ASIC, 1996. 2nd International Conference on
21-24 Oct. 1996 Page(s):239 - 242
Digital Object Identifier 10.1109/ICASIC.1996.562797
AbstractPlus | Full Text: PDF(328 KB) **IEEE CNF**

☐ **7. Radiation Qualification of Electronics Components Used for Level-1 Muon Endcap Trigger System**
Ichimiya, R.; Tsuji, S.; Arai, Y.; Ikeno, M.; Sasaki, O.; Ohshita, H.; Hane, Y.; Hasuko, K.; Nomoto, H.; Sakamoto, H.; Shibuya, K.; Ta Fukunaga, C.; Toshima, K.; Sakuma, T.;
Nuclear Science, IEEE Transactions on
Volume 52, Issue 4, Aug. 2005 Page(s):1061 - 1066
Digital Object Identifier 10.1109/TNS.2005.852700
AbstractPlus | Full Text: PDF(536 KB) **IEEE JNL**

☐ **8. Radiation qualification of electronics components used for tl level-1 muon endcap trigger system**
Ichimiya, R.; Tsuji, S.; Arai, Y.; Ikeno, M.; Sasaki, O.; Ohshita, H.; Hane, Y.; Hasuko, K.; Nomoto, H.; Sakamoto, H.; Shibuya, K.; Ta Fukunaga, C.; Toshima, K.; Sakuma, T.;
Nuclear Science Symposium Conference Record, 2004 IEEE
Volume 2, 16-22 Oct. 2004 Page(s):779 - 783 Vol. 2
Digital Object Identifier 10.1109/NSSMIC.2004.1462325
AbstractPlus | Full Text: PDF(981 KB) **IEEE CNF**

☐ **9. LSP speech synthesis ASIC architecture**
Xingjun Wu; Yihe Sun;
Solid-State and Integrated Circuit Technology, 1995 4th Internatic Conference on
24-28 Oct. 1995 Page(s):700 - 702
Digital Object Identifier 10.1109/ICSICT.1995.503532
AbstractPlus | Full Text: PDF(156 KB) **IEEE CNF**

☐ **10. Integrated FPGA based ASIC design on error code correctio UPS telecommunication**
Jian-Long Kuo; Chin-Chin Tsai; Lai, L.F.; Chen, T.J.; Ding, T.W.;
Power Electronics and Drive Systems, 2001. Proceedings., 2001 International Conference on
Volume 2, 22-25 Oct. 2001 Page(s):512 - 516 vol.2
AbstractPlus | Full Text: PDF(385 KB) **IEEE CNF**

☐ **11. A full-parallel digital implementation for pre-trained NNs**
Szabo, T.; Antoni, L.; Horvath, G.; Feher, B.;
Neural Networks, 2000. IJCNN 2000, Proceedings of the IEEE-IN International Joint Conference on
Volume 2, 24-27 July 2000 Page(s):49 - 54 vol.2
Digital Object Identifier 10.1109/IJCNN.2000.857873
AbstractPlus | Full Text: PDF(456 KB) **IEEE CNF**

☐ **12. Efficient implementation of a serial/parallel multiplier for IP b development and rapid prototyping in VLSI digital signal pro**
Adaos, K.D.; Alexiou, G.P.; Kanopoulos, N.;

Electronics, Circuits and Systems, 1999. Proceedings of ICECS '
IEEE International Conference on
Volume 1, 5-8 Sept. 1999 Page(s):33 - 36 vol.1
Digital Object Identifier 10.1109/ICECS.1999.812217
AbstractPlus | Full Text: PDF(196 KB) **IEEE CNF**

☐ **13. Performance characteristics of a new generation of processi for PET applications**
Musrock, M.S.; Young, J.W.; Moyers, J.C.; Breeding, J.E.; Casey Rochelle, J.M.; Binkley, D.M.; Swann, B.K.;
Nuclear Science Symposium Conference Record, 2002 IEEE
Volume 1, 10-16 Nov. 2002 Page(s):101 - 105 vol.1
AbstractPlus | Full Text: PDF(337 KB) **IEEE CNF**

☐ **14. RISC system design in an FPGA**
Luker, J.D.; Prasad, V.B.;
Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 2001 Midwest Symposium on
Volume 2, 14-17 Aug. 2001 Page(s):532 - 536 vol.2
Digital Object Identifier 10.1109/MWSCAS.2001.986247
AbstractPlus | Full Text: PDF(195 KB) **IEEE CNF**

☐ **15. SDR-based digital channelizer/de-channelizer for multiple Cl**
Chonghoon Kim; Yoan Shin; Sungbin Im; Woncheol Lee;
Vehicular Technology Conference, 2000. IEEE VTS-Fall VTC 20
Volume 6, 24-28 Sept. 2000 Page(s):2862 - 2869 vol.6
Digital Object Identifier 10.1109/VETECF.2000.886841
AbstractPlus | Full Text: PDF(676 KB) **IEEE CNF**

☐ **16. Development of a data acquisition system for the MiCES sm PET scanner**
Lewellen, T.K.; Laymon, C.M.; Miyaoka, R.S.; Janes, M.; Byungk Lee; Kinahan, P.E.;
Nuclear Science Symposium Conference Record, 2002 IEEE
Volume 2, 10-16 Nov. 2002 Page(s):1066 - 1070 vol.2
Digital Object Identifier 10.1109/NSSMIC.2002.1239506
AbstractPlus | Full Text: PDF(388 KB) **IEEE CNF**

☐ **17. A FPGA-based implementation of data acquisition and proce digital protective relays**
Feng Tao; Zhang Guiqing; Wang Jianhua; Geng Yingsan; Zhang
ASIC, 2001. Proceedings. 4th International Conference on
23-25 Oct. 2001 Page(s):518 - 521
Digital Object Identifier 10.1109/ICASIC.2001.982614
AbstractPlus | Full Text: PDF(368 KB) **IEEE CNF**

☐ **18. Low power, area efficient programmable filter and variable r**
Grayver, E.; Daneshrad, B.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. IEEE International Symposium on
Volume 5, 28-31 May 2000 Page(s):341 - 344 vol.5
Digital Object Identifier 10.1109/ISCAS.2000.857434
AbstractPlus | Full Text: PDF(368 KB) **IEEE CNF**

☐ **19. XCC-a tool for designing parameterizable IP cores in VHDL**
Mitra, S.;
Signals, Systems, and Computers, 1999. Conference Record of Third Asilomar Conference on
Volume 1, 24-27 Oct. 1999 Page(s):752 - 756 vol.1

Digital Object Identifier 10.1109/ACSSC.1999.832429
AbstractPlus | Full Text: PDF(400 KB) **IEEE CNF**

☐ **20. Resonator based digital filters using field programmable gat elements**
Feher, B.;
ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annua International
21-25 Sept. 1992 Page(s):119 - 122
Digital Object Identifier 10.1109/ASIC.1992.270294
AbstractPlus | Full Text: PDF(416 KB) **IEEE CNF**

☐ **21. Efficient design of application specific DSP cores using FPG**
Attri, S.; Sohi, B.S.; Chopra, Y.C.;
ASIC, 2001. Proceedings. 4th International Conference on
23-25 Oct. 2001 Page(s):462 - 466
Digital Object Identifier 10.1109/ICASIC.2001.982600
AbstractPlus | Full Text: PDF(524 KB) **IEEE CNF**

☐ **22. Neural network implementation using distributed arithmetic**
Szabo, T.; Feher, B.; Horvath, G.;
Knowledge-Based Intelligent Electronic Systems, 1998. Proceed 1998 Second International Conference on
Volume 3, 21-23 April 1998 Page(s):510 - 518 vol.3
Digital Object Identifier 10.1109/KES.1998.726016
AbstractPlus | Full Text: PDF(696 KB) **IEEE CNF**

☐ **23. An SDH STM-1 termination IC**
Zhang Xiaoru; Zeng Lieguang;
ASIC, 1996. 2nd International Conference on
21-24 Oct. 1996 Page(s):179 - 182
Digital Object Identifier 10.1109/ICASIC.1996.562781
AbstractPlus | Full Text: PDF(292 KB) **IEEE CNF**

☐ **24. A Java processor suitable for applications of smart card**
Zhang Jianjie; Li Feihui; Ge Yuanqing; Yue Zhenwu; Yang Zhilia
ASIC, 2001. Proceedings. 4th International Conference on
23-25 Oct. 2001 Page(s):736 - 739
Digital Object Identifier 10.1109/ICASIC.2001.982668
AbstractPlus | Full Text: PDF(318 KB) **IEEE CNF**

[redacted]

Help Contac
Secu

Indexed by Inspec